CLAIMS

Having thus described our invention in detail, what we claim as new is:

1. A method of fabricating a microstructure comprising the steps of:

providing a structure comprising a multi-layered stack located atop an etchable material, said multi-layered stack comprising a core material including at least one diffusing element located between top and bottom diffusion barrier layers;

patterning the multi-layered stack to provide a plurality of patterned multi-layered stacks on the etchable material, each patterned multi-layered stack having etched facets;

heating the patterned multi-layered stacks to cause lateral diffusion of the at least one diffusing element to the etched facets;

removing the at least one diffusing element from the etched facets; and

performing a self-correcting dopant-sensitive etching process on a plurality of exposed patterned multi-layered stack to provide patterned lines that have a substantially reduced line width and substantially reduced line width variation.

2. The method of Claim 1 wherein said core material comprises a doped glass, doped silicon, or a doped polymer-based material.

3. The method of Claim 1 wherein the top and bottom barrier layers are the same or different and comprise a silicon nitride, a metal nitride or a metal oxynitride.

4. The method of Claim 1 wherein said patterning of the multi-layered stack includes photolithography and etching.

5. The method of Claim 1 wherein said heating is performed at a temperature of from about 100°C to about 1200°C.

6. The method of Claim 1 wherein the at least one diffusing element is removed from the etched facets by an evaporation process.

7. The method of Claim 6 wherein the evaporation process includes a gaseous phase about the structure.

8. The method of Claim 6 wherein the evaporation process is performed in the presence of a reactive ambient or a neutral ambient.

9. The method of Claim 1 wherein the at least one diffusing element is removed using a gettering material that is applied adjacent to the etched facets.

10. The method of claim 1 further comprising a step of covering a subset of patterned features with a block mask to expose only a plurality of select lines, said covering step is performed between said removing and said self-correcting etching process.

11. The method of Claim 1 wherein the self-correcting etching removes highly doped patterned multi-layered stacks at a faster rate than lightly doped patterned multi-layered stacks.

12. The method of Claim 1 wherein the self-correcting etching removes wider patterned multi-layered stacks at a faster rate than narrower patterned multi-layered stacks.

13. The method of Claim 1 wherein the etchable material is a gate conductor.

14. The method of Claim 1 further comprising forming a diffusion barrier about each etched facet prior to performing the self-correcting etching process.

15. The method of claim 1 further comprising performing an additional etching step after said self-correcting etching process, said additional etching step removes underlying etchable material.

16. The method of claim 1 wherein the lateral diffusion has a characteristic diffusion length range from about one forth of the nominal line width to about the nominal line width.

17. A microstructure comprising:

a plurality of one-dimensional structures, each having a critical dimension L that it is less than a minimal feature size F obtainable by lithography, or any either patterning, etching, deposition or shaping technique, wherein the plurality of structures have a variation in critical dimension that is less than the $\Delta L \cdot F/L$, where ΔL is the range of critical dimension variation obtainable by lithography or any other patterning, etching, deposition, or shaping technique which forms microstructure with minimal feature size F.

18. The microstructure of Claim 17 wherein the plurality of structures are one-dimensional structures which satisfy the following:

$$\mathbf{var}(L_{max} - L_{min}) < 0.5\ \mathbf{var}(L_{ave}) = \sigma_L < 5\%, \quad (1)$$

where L_{max}, L_{min}, L_{ave} are maximum, minimal, and average value of L for each structure and **var** is a symbol for standard deviation of a random function; and

$$\mathbf{var}(V) < 1.67\ \mathbf{var}(L_{ave}) = 1.67\sigma_L, \quad (2)$$

where V is the structure volume.

19. The microstructure of Claim 17 wherein the plurality of structures are gates of a CMOS device, cylinders or disks.

20. The microstructure of Claim 17 wherein the plurality of structures are parallel periodic lines having a width L and a spatial period equal to or less than 2F, and variation of spacing between adjacent line substantially equal to the variation of distance between adjacent line centers, the line centers being the line middle point in the width direction.